#4

Form 1449*	Atty. Docket No.: 884.141US1	Serial No. 09/431,477
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Kiran Ganesh et al.	
	Filing Date: Herewith	Group: 2825

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	No

OTHER DOCUMENTS
(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
PC	Basaran, B., et al., "GeneSys: A Leaf-Cell Layout Synthesis System for GHz VLSI Designs", Proceedings of the 12th International Conference on VLSI Design, 448-452, (Jan. 1999)
PC	Gupta, A., et al., "CLIP: An Optimizing Layout Generator for Two-Dimensional CMOS Cells", Proceedings of the 34th Design Automation Conference, 452-455, (June 1997)
PC	Gupta, A., et al., "Near-Optimum Hierarchical Layout Synthesis of Two-Dimensional CMOS Cells", Proceedings of the 12th International Conference on VLSI Design, 453-459, (Jan. 1999)
PC	Gupta, A., et al., "Width Minimization of Two-Dimensional CMOS Cells Using Integer Programming", Proceedings of the IEEE/ACM International Conference on CAD, 660-667, (1996)
PC	Ho, J., et al., "New Algorithms for the Rectilinear Steiner Tree Problem", IEEE Transactions on Computer-Aided Design, Vol. 9, 185-193, (Feb. 1990)
PC	Hsieh, Y., et al., "LiB: A CMOS Cell Compiler", IEEE Transactions on Computer-Aided Design, Vol. 10, 994-1005, (Aug. 1991)
PC	Hu, C., et al., "Electromigration Under Bidirectional Current Stress", Proceedings of the Symposium on Reliability of Metals in Electronics, 188-202, (1995)
PC	Hwang, C.Y., et al., "An Efficient Layout Style for Two-Metal CMOS Leaf Cells and Its Automatic Synthesis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, 410-424, (March 1993)
PC	Riepe, M.A., et al., "Transistor Level Micro Placement and Routing for Two-Dimensional Digital VLSI Cell Synthesis", Technical Report CSE-TR-364-98, The University of Michigan, Ann Arbor, 1-18, (June 1998)

Examiner Phallaka Kib	Date Considered 9/13/01

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*	Atty. Docket No.: 884.141US1	Serial No. ~~Unknown~~ 09/431,477
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Kiran Ganesh et al.	
	Filing Date: Herewith	Group: ~~Unknown~~ 2825

OTHER DOCUMENTS

**Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Etc.)
PD	Romeo, F., et al., "Research on Simulated Annealing at Berkeley", Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers, 652-657, (Oct. 1984)
PD	Saika, S., et al., "A Two-Dimensional Transistor Placement Algorithm for Cell Synthesis and Its Application to Standard Cells", IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Vol.E80-A, 1883-1891, (Oct. 1997)
PD	Tani, K., et al., "Two-Dimensional Layout Synthesis for Large-Scale CMOS Circuits", IEEE Internaltional Conference on Computer-Aided Design, 490-493, (Nov. 1991)
PD	Wimer, S., et al., "Optimal Chaining of CMOS Transistors in a Functional Cell", IEEE Transactions on Computer-Aided Design, Vol. CAD-6, 795-801, (Sept. 1987)

Examiner Phallaka Kik	Date Considered 9/18/2001

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.